REMARKS

Claims 1 and 11 have been amended. Claims 24-34 were previously canceled without prejudice to the underlying subject matter. Claims 1-23 and 35-40 are currently pending in this application.

Applicants graciously acknowledge the allowance of claims 19-23.

Claims 1-18 and 35-38 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Yoon et al., US Patent No. 6,479,887 (Yoon). This rejection is respectfully traversed.

The claimed invention relates to a method of packaging semiconductor devices. Independent claim 1 recites a "method of making semiconductor device packages" comprising, *inter alia*, "testing semiconductor devices in said wafer" and "subsequently, dicing said layered assembly." As amended, independent claim 11 recites a "method of making semiconductor device packages" comprising, *inter alia*, "determining whether the wafer contains a defective semiconductor device" and "subsequently, dicing said layered assembly." Independent claim 35 recites a "method of handling a plurality of semiconductor devices arrayed in a semiconductor wafer" comprising, *inter alia* "testing said semiconductor devices through said ball grid arrays."

Yoon relates to a circuit pattern tape that eliminates wafer chipping during package singulation by using a resin envelope formation region on the tape that does not intersect the singulation lines of the tape and wafer. Yoon, however, fails to disclose all limitations of any of independent claims 1, 11, and 35. Specifically, Yoon fails to disclose the above noted limitations of claims 1, 11, and 35.

The Examiner asserts that Yoon discloses testing semiconductor devices in a wafer and testing semiconductor devices through ball grid arrays. Office Action at 3 and 5. Applicants respectfully disagree. Yoon discloses that there are test regions 27 for testing

the circuit pattern tape 10. Yoon does not mention testing of any semiconductor devices in a wafer. Notably, Yoon states that processes for forming semiconductor packages are either not performed on the test regions 27; or, if performed, the packages resulting from the test regions 27 are discarded. Yoon at col. 11, lines 60-65. Further, Yoon is silent about when testing of the circuit pattern tape occurs. Accordingly, while Yoon does disclose testing the circuit pattern tape, Yoon does not disclose testing "semiconductor devices in said wafer," as recited by independent claim 1; "determining whether the wafer contains a defective semiconductor package," as recited by independent claim 11; or "semiconductor devices arrayed in a wafer," as recited by independent claim 35.

Claims 39 and 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoon in view of Miyawaki, US Patent No. 6,268,236 (Miyawaki). This rejection is respectfully traversed.

As discussed above, Yoon fails to disclose, teach, or suggest all limitations of independent claim 35, from which claims 39 and 40 depend. Miyawaki does not supplement the deficiencies of Yoon. Instead, Miyawaki is cited for teaching the step of attaching a dielectric tape to an assembly by applying heat or pressure and evacuating gas from the assembly. Accordingly, for at least these reasons, withdrawal of this rejection is respectfully requested.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: December 22, 2004

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Elizabeth Parsons
Registration No.: 52,499
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicants